TED (10) –3066

Reg. No.....

(REVISION — 2010)

Signature .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — OCTOBER, 2017

DIGITAL COMPUTER PRINCIPLES

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Convert binary 11010 to decimal.
2. What is don't care condition ?
3. List the applications of multiplexer.
4. Define latch.
5. Define max term. (5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Explain ASCII and EBCDIC.
2. Convert :
   (a) decimal 251 to octal.
   (b) hex B9 to decimal.
3. Explain any 3 logic families.
4. Explain half subtractor with diagram.
5. Design a 4 × 1 multiplexer.
6. Construct SR flip-flop using NAND gates.
7. Compare synchronous and asynchronous sequential logic circuits. (5×6 = 30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III Draw truth tables and symbols of logic gates. 15

OR

IV (a) Explain sum of product and product of sum with examples. 8

(b) Explain BCD. 7

UNIT — II

V Solve using K-maps $F(w,x,y,z) = \sum(1,3,7,11,15)$ with don't care conditions $d(w,x,y,z) = \sum(0,2,5)$ 15

OR

VI (a) Write short note on fan-in, fan-out and Noise margin. 9

(b) Draw k-map for xy+x'y'z'+xiyz'. 6

UNIT — III

VII (a) Explain about serial and parallel adders. 8

(b) Explain a BCD to decimal decoder. 7

OR

VIII (a) Design a full adder circuit. 8

(b) Explain de-multiplexer. 7

UNIT — IV

IX (a) Explain JK flip-flop with its truth table. 8

(b) Explain the working of "parallel in serial out" and "parallel in parallel out" shift registers. 7

OR

X (a) Compare sequential and combinational circuits. 8

(b) Explain the ring counter. 7

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